

## (SCHEME OF EXAMINATIONS)

Scheme of Programme Code: 052      Programme Name: MASTER OF TECHNOLOGY (VLSI DESIGN)      SchemeID: 310522015001      Sem./Year: 01 SEMESTER  
Institution Code: 118      Institution: C-DAC, NOIDA

S.No.	Paper ID	Code	Subject	Credit	Type	Exam	Mode	Kind	Minor	Major	Max. Marks	Pass Marks
01	52601	MEVS601	DIGITAL SYSTEM DESIGN USING VERILOG	4	THEORY	UES	COMPULSORY	DROPPABLE	25	75	100	40
02	52603	MEVS603	VLSI TECHNOLOGY	4	THEORY	UES	COMPULSORY	DROPPABLE	25	75	100	40
03	52605	MEVS605	ADVANCED VLSI DESIGN	4	THEORY	UES	COMPULSORY	DROPPABLE	25	75	100	40
04	48607	MECS607	ADVANCED COMPUTER ARCHITECTURE	4	THEORY	UES	ELECTIVE	DROPPABLE	25	75	100	40
05	52609	MEVS609	ALGORITHM ANALYSIS AND DESIGN	4	THEORY	UES	ELECTIVE	DROPPABLE	25	75	100	40
06	48611	MECS611	COMPUTATIONAL TECHNIQUES USING MATLAB	4	THEORY	UES	ELECTIVE	DROPPABLE	25	75	100	40
07	52611	MEVS611	DSP FOR VLSI DESIGN	4	THEORY	UES	ELECTIVE	DROPPABLE	25	75	100	40
08	52613	MEVS613	WIRELESS NETWORKS	4	THEORY	UES	ELECTIVE	DROPPABLE	25	75	100	40
09	52615	MEVS615	RESEARCH METHODOLOGIES	4	THEORY	UES	ELECTIVE	DROPPABLE	25	75	100	40
10	52651	MEVS651	LAB-1 (DSD LAB)	1	PRACTICAL	UES	COMPULSORY	DROPPABLE	40	60	100	40
11	52653	MEVS653	LAB-2 (VLSI TECH. LAB)	1	PRACTICAL	UES	COMPULSORY	DROPPABLE	40	60	100	40
12	52655	MEVS655	LAB-3 (AD. VLSI LAB)	1	PRACTICAL	UES	COMPULSORY	DROPPABLE	40	60	100	40
13	52657	MEVS657	TERM PAPER-I	2	PRACTICAL	NUES	COMPULSORY	DROPPABLE	--	100	100	40



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S.No.	Paper ID	Code	Subject	Credit	Type	Exam	Mode	Kind	Minor	Major	Max. Marks	Pass Marks
01	52701	MEVS701	ALGORITHM FOR VLSI PHYSICAL DESIGN AUTOMATION	4	THEORY	UES	COMPULSORY	DROPPABLE	25	75	100	40
02	52703	MEVS703	VLSI DESIGN TEST AND TESTABILITY	4	THEORY	UES	COMPULSORY	DROPPABLE	25	75	100	40
03	42705	MEEC705	EMBEDDED SYSTEMS & RTOS	4	THEORY	UES	ELECTIVE	DROPPABLE	25	75	100	40
04	52705	MEVS705	ANALOG-MIXED SIGNAL DESIGN	4	THEORY	UES	ELECTIVE	DROPPABLE	25	75	100	40
05	52707	MEVS707	HARDWARE-SOFTWARE CO-DESIGN	4	THEORY	UES	ELECTIVE	DROPPABLE	25	75	100	40
06	52709	MEVS709	DESIGNING WITH FPGA	4	THEORY	UES	ELECTIVE	DROPPABLE	25	75	100	40
07	52711	MEVS711	ADVANCED DIGITAL COMMUNICATION SYSTEM	4	THEORY	UES	ELECTIVE	DROPPABLE	25	75	100	40
08	52713	MEVS713	MEMS AND IC INTEGRATION	4	THEORY	UES	ELECTIVE	DROPPABLE	25	75	100	40
09	52715	MEVS715	NETWORK ON CHIP DESIGN	4	THEORY	UES	ELECTIVE	DROPPABLE	25	75	100	40
10	52717	MEVS717	CMOS RF DESIGN	4	THEORY	UES	ELECTIVE	DROPPABLE	25	75	100	40
11	52719	MEVS719	CIRCUIT INTERCONNECTIONS AND PACKAGING FOR VLSI	4	THEORY	UES	ELECTIVE	DROPPABLE	25	75	100	40
12	52751	MEVS751	LAB-7 (ALGO. VLSI PDA LAB)	1	PRACTICAL	UES	COMPULSORY	DROPPABLE	40	60	100	40
13	52753	MEVS753	LAB-8 (VDTT LAB)	1	PRACTICAL	UES	COMPULSORY	DROPPABLE	40	60	100	40
14	52755	MEVS755	TERM PAPER III	2	PRACTICAL	NUES	COMPULSORY	DROPPABLE	--	100	100	40
15	52757	MEVS757	MINOR PROJECT	4	PRACTICAL	UES	COMPULSORY	DROPPABLE	40	60	100	40







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01	52601	MEVS601	DIGITAL SYSTEM DESIGN USING VERILOG	4	THEORY	UES	COMPULSORY	DROPPABLE	25	75	100	40
02	52603	MEVS603	VLSI TECHNOLOGY	4	THEORY	UES	COMPULSORY	DROPPABLE	25	75	100	40
03	52605	MEVS605	ADVANCED VLSI DESIGN	4	THEORY	UES	COMPULSORY	DROPPABLE	25	75	100	40
04	48607	MECS607	ADVANCED COMPUTER ARCHITECTURE	4	THEORY	UES	ELECTIVE	DROPPABLE	25	75	100	40
05	52609	MEVS609	ALGORITHM ANALYSIS AND DESIGN	4	THEORY	UES	ELECTIVE	DROPPABLE	25	75	100	40
06	48611	MECS611	COMPUTATIONAL TECHNIQUES USING MATLAB	4	THEORY	UES	ELECTIVE	DROPPABLE	25	75	100	40
07	52611	MEVS611	DSP FOR VLSI DESIGN	4	THEORY	UES	ELECTIVE	DROPPABLE	25	75	100	40
08	52613	MEVS613	WIRELESS NETWORKS	4	THEORY	UES	ELECTIVE	DROPPABLE	25	75	100	40
09	52615	MEVS615	RESEARCH METHODOLOGIES	4	THEORY	UES	ELECTIVE	DROPPABLE	25	75	100	40
10	52651	MEVS651	LAB-1 (DSD LAB)	1	PRACTICAL	UES	COMPULSORY	DROPPABLE	40	60	100	40
11	52653	MEVS653	LAB-2 (VLSI TECH. LAB)	1	PRACTICAL	UES	COMPULSORY	DROPPABLE	40	60	100	40
12	52655	MEVS655	LAB-3 (AD. VLSI LAB)	1	PRACTICAL	UES	COMPULSORY	DROPPABLE	40	60	100	40
13	52657	MEVS657	TERM PAPER-I	2	PRACTICAL	NUES	COMPULSORY	DROPPABLE	--	100	100	40







LEGEND

PAPERID (CREDITS)	
Internal	External
TOTAL (GRADE)	

A: Absent C: Cancelled  
 D: Detained RL: Result Later  
 CS: Credits Secured  
 AP: Already Passed

Result of Programme Code: 052 Programme Name: MASTER OF TECHNOLOGY (VLSI DESIGN) Sem./Year: 01 SEMESTER Batch: 2016 Examination: REGULAR December, 2016

S.No.	Photo.	Roll no./Name	Institution Code: 118 Institution: C-DAC, NOIDA																				CS/Remarks														
			52601 (4)	52603 (4)		52605 (4)		48607 (4)		52609 (4)		52651 (1)		52653 (1)		52655 (1)		52657 (2)																			
21		02611805216 DITIPRIYA BANERJEE SID: 310000013483 SchemeID: 310522015001	17	59	19	61	19	55	22	65	20	51	34	51	33	49	34	54	-	80																25	
			76 (A+)		80 (A+)		74 (A)		87 (A+)		71 (A)		85 (A+)		82 (A+)		88 (A+)		80 (A+)																		
22		02711805216 AJAY MALL SID: 310000013484 SchemeID: 310522015001	14	49	17	46	22	54	17	55	17	39	33	46	33	48	31	42	-	70																25	
			63 (B+)		63 (B+)		76 (A+)		72 (A)		56 (B+)		79 (A+)		81 (A+)		73 (A)		70 (A)																		
23		02811805216 DISHA TANWAR SID: 310000013485 SchemeID: 310522015001	18	54	17	56	16	44	18	57	19	44	34	44	33	51	35	50	-	67																25	
			72 (A)		73 (A)		60 (B+)		75 (A+)		63 (B+)		78 (A+)		84 (A+)		85 (A+)		67 (A)																		
24		02911805216 VINAY MISHRA SID: 310000013486 SchemeID: 310522015001	20	61	16	33	22	48	16	50	20	39	37	54	34	49	36	48	-	84																25	
			81 (A+)		49 (C)		70 (A)		66 (A)		59 (B+)		91 (O)		83 (A+)		84 (A+)		84 (A+)																		
25																																					
26																																					
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28																																					
29																																					
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\*Passed with Grace Marks  
 \*SID: Student ID; SchemeID: The scheme applicable to the student.  
 Date on which pdf made: 19/04/2017  
 RTSID: 2017041905220161180010